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a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment;

a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication.

2. (Amended) The processor as recited in claim 1 wherein said default address size is a first address size if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said default address size is a second address size if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. (Amended) The processor as recited in claim 2 wherein said second address size is one of a plurality of address sizes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

4. (Amended) The processor as recited in claim 3 wherein one of said plurality of address sizes is a 32 bit address size.

5. (Amended) The processor as recited in claim 3 wherein one of said plurality of address sizes is a 16 bit address size.

6. (Amended) The processor as recited in claim 2 wherein said first address size is

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greater than 32 bits.

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10. (Amended) The processor as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said processor is configured to establish said default address size responsive to said second operating mode indication.

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~~17~~. (Amended) A method comprising:

establishing a default address size in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, said segment descriptor further including one or more bits identifying a segment described by said segment descriptor as a code segment; and

generating addresses of said default address size.

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~~18~~. (Amended) The method as recited in claim ~~17~~ wherein said establishing comprises establishing a first address size responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first address size is greater than 32 bits.

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~~21~~. (Twice Amended) The method as recited in claim ~~18~~ wherein said establishing further comprises establishing a second address size responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second address size is 32 bits.

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~~22~~. (Amended) The method as recited in claim ~~18~~ wherein said establishing further comprises establishing one of a plurality of address sizes if said enable indication is in